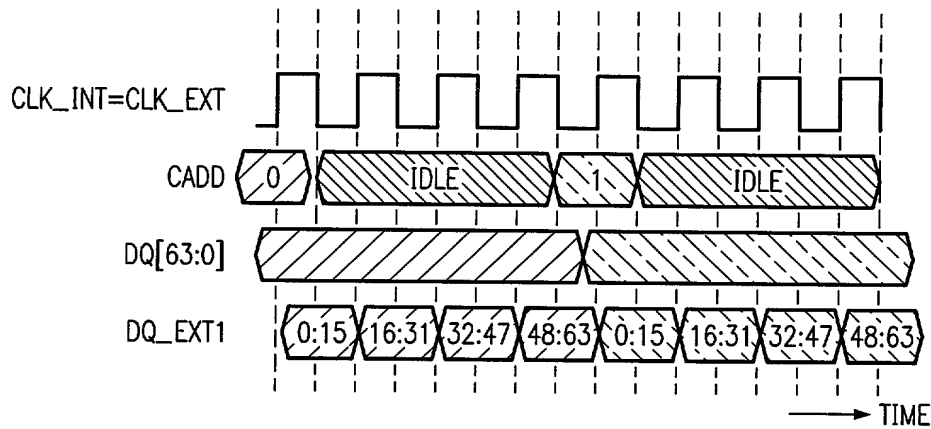


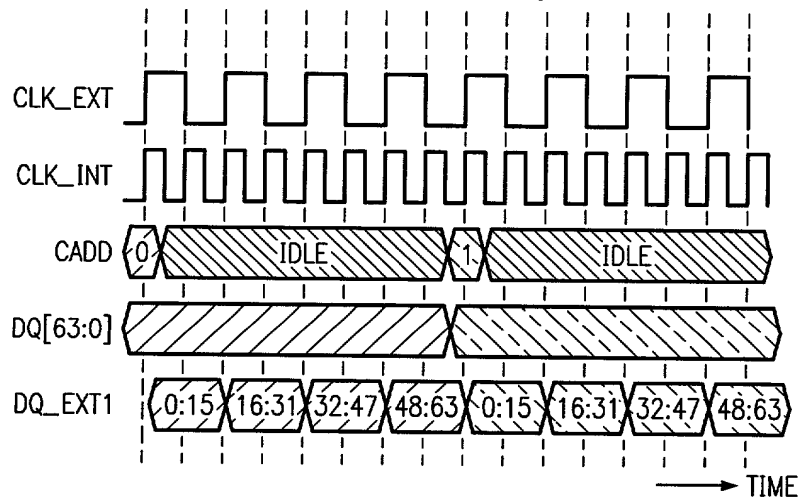
1/6

**FIG. 1**  
(PRIOR ART)



Data read sequence for a 64 bit data bus and a 16 bit wide external tester interface (internal clock frequency= external clock frequency). Note that between each read operation the eDRAM will stay for 3 cycles in idle mode.

**FIG. 2**  
(PRIOR ART)



Data read sequence for a 64 bit data bus and a 16 bit wide external tester interface (internal clock frequency= 2x external clock frequency). Note that between each read operation the eDRAM will stay for 7 cycles in idle mode.

2/6

FIG. 3

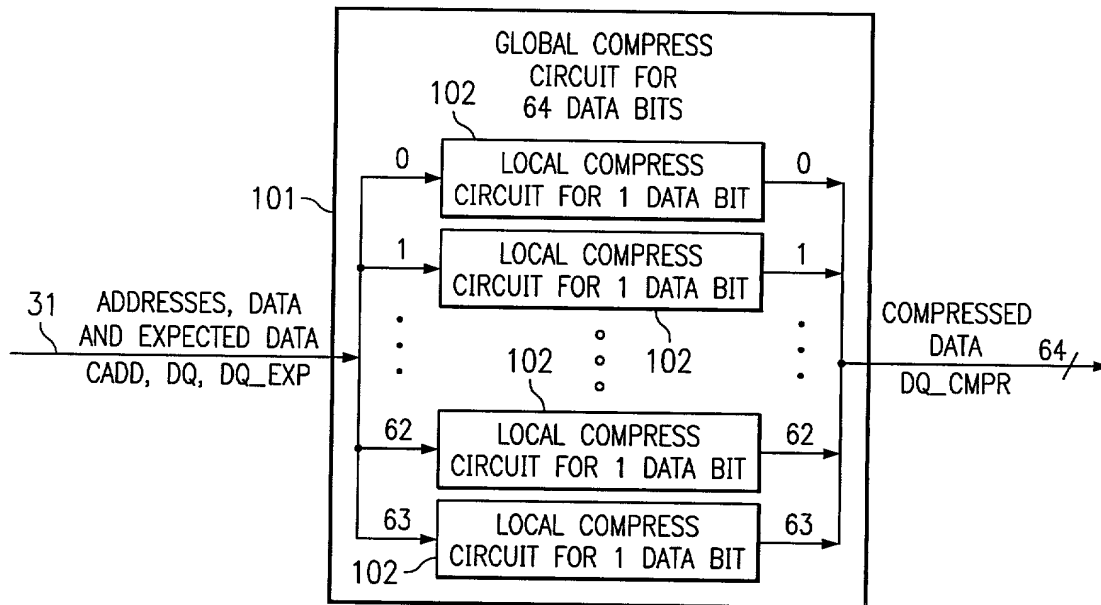
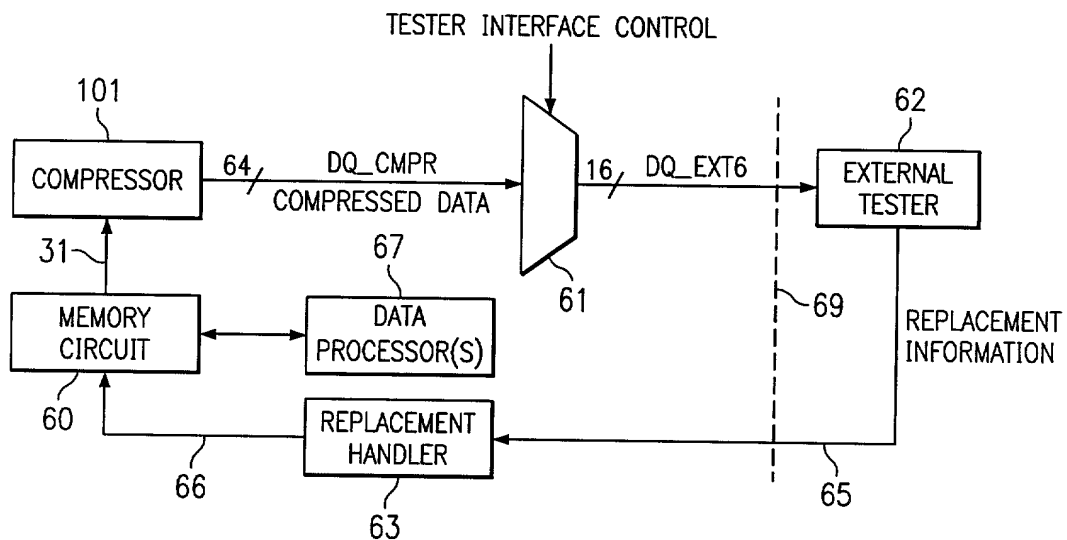
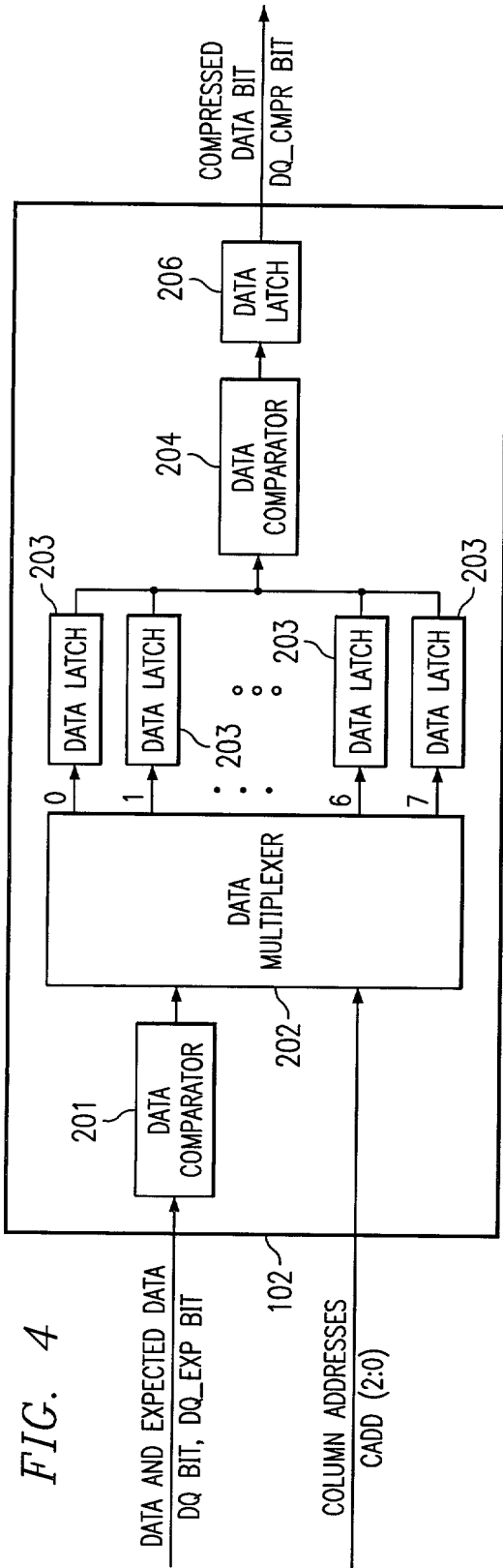
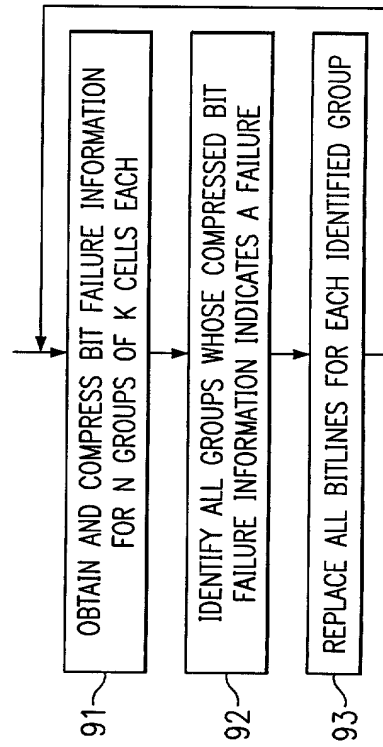


FIG. 6



3/6

**FIG. 9**

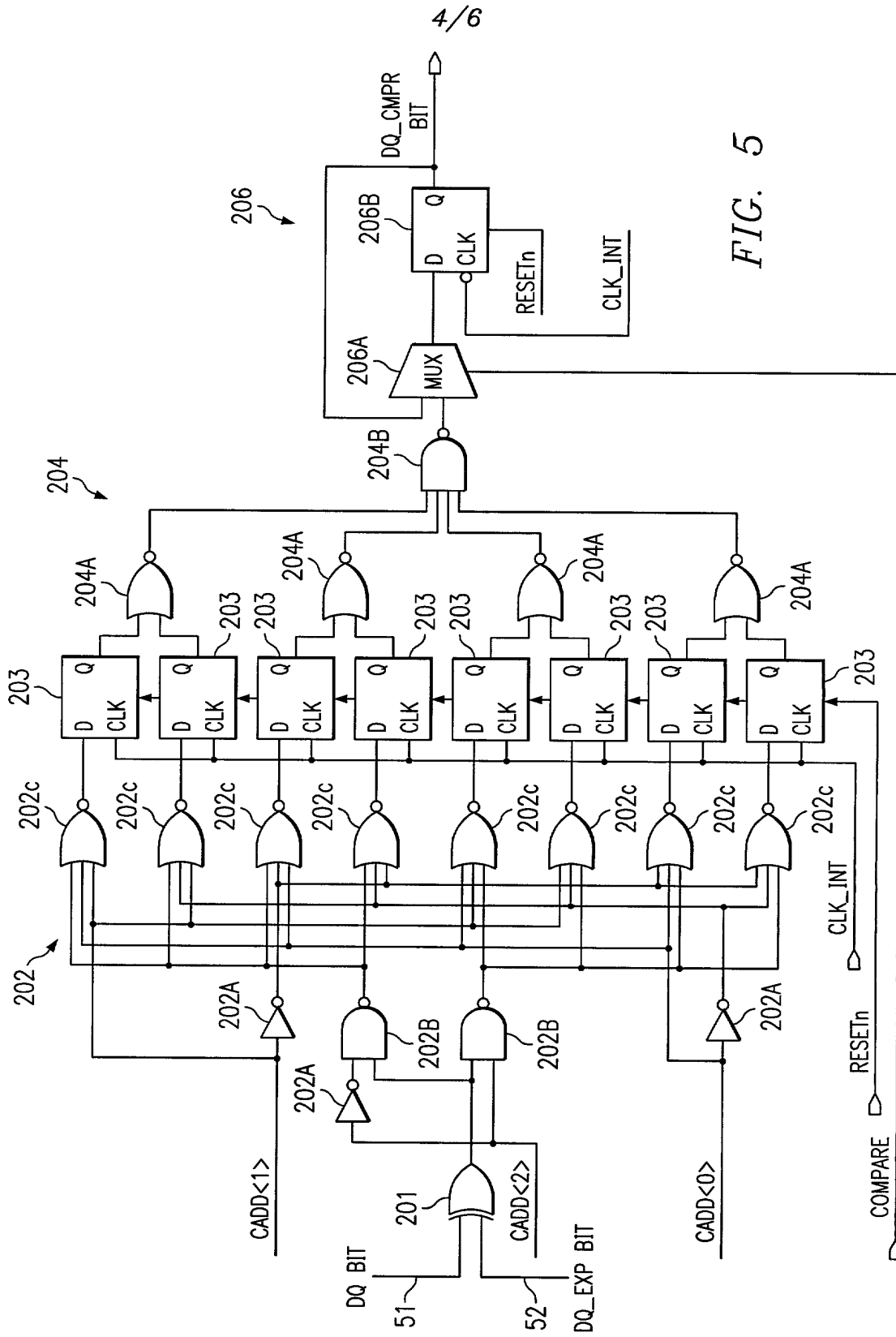
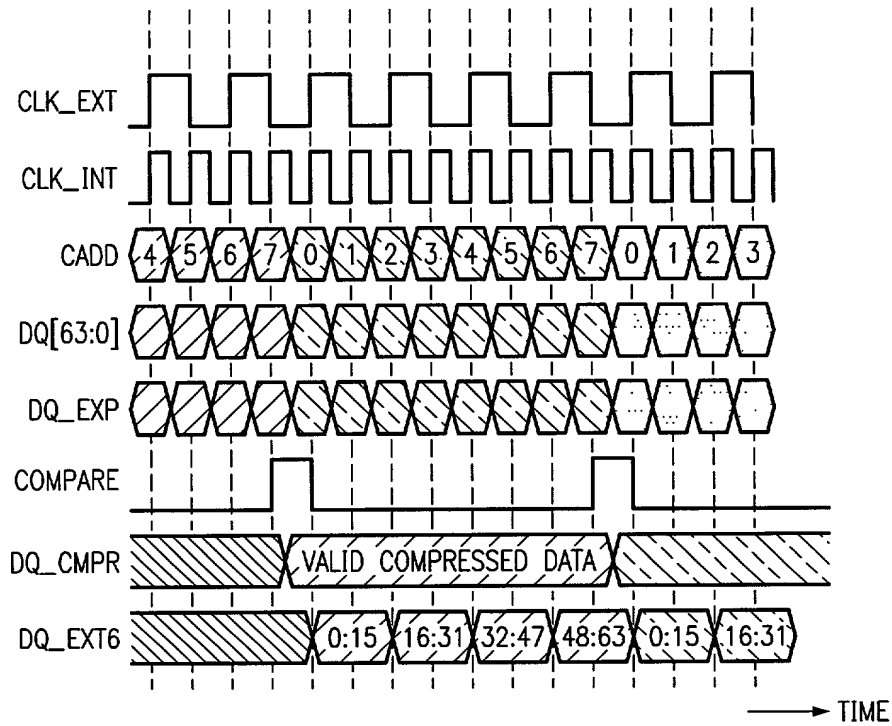


FIG. 5

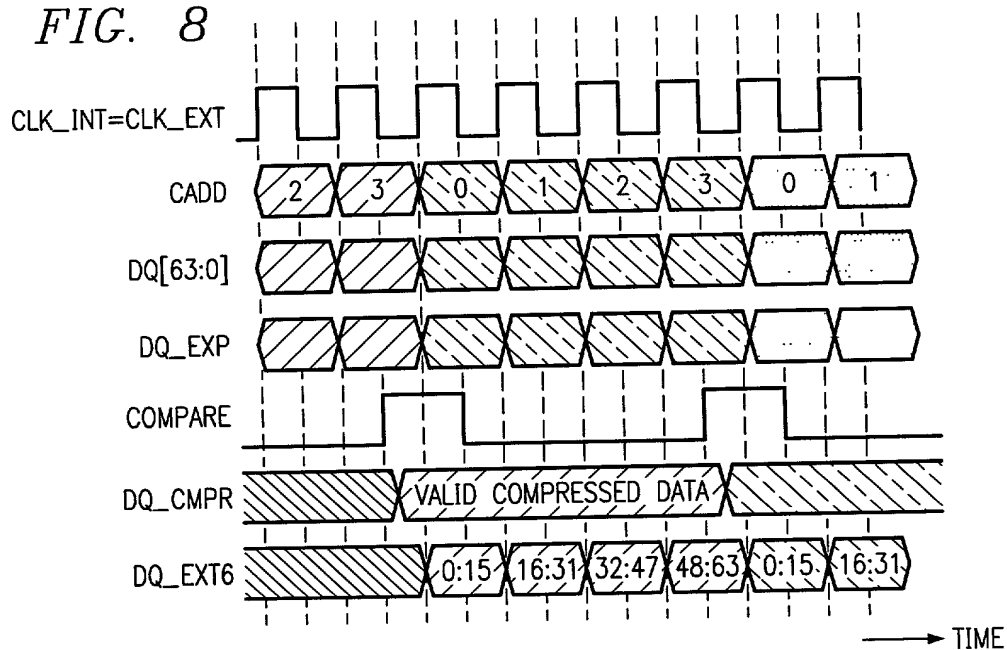
5/6

FIG. 7



Data read sequence for a 64 bit data bus and a 16 bit wide external tester interface (internal clock frequency=2x external clock frequency). Note that the time for multiplexing the compressed data (from previous read cycles) to the tester is used to compress the current read data. No cycles are lost, 8 bit compression.

FIG. 8



Data read sequence for a 64 bit data bus and a 16 bit wide external tester interface (internal clock frequency=external clock frequency). Note that the time for multiplexing the compressed data (from previous read cycles) to the tester is used to compress current read data. No cycles are lost, 4 bit compression.